ABSTRACT OF THE DISCLOSURE

First and second latch circuits store "0" and "1", respectively, by reset. An output signal from the first latch circuit is input to the second latch circuit. Register setting data is input to the first latch circuit via a first gate that allows an input signal to pass through when the output signal from the second latch circuit is "1", and outputs "0" when the output signal from the second latch circuit is "0". A write signal is supplied to a memory via a second gate that allows the input signal to pass through only when the output signal from the first latch circuit is "1". When the register setting data indicates "0", the output signals from both the first and the second latch circuits become "0", and until being reset, the write error protect state is maintained.